Day 3 (Poster E)

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Title: Quantitative Evaluation of an FPGA-Based SQA Accelerator Exploiting Trotter-Slice Parallelism

Abstract:
Quantum annealing (QA) is a heuristic to solve combinatorial optimization problems using quantum fluctuations. For large problems that are hard to be handled on a real annealer，simulated quantum annealing (SQA) is known as an alternative. Previous FPGA-based SQA accelerators shows that multiple Trotter slices can be processed in parallel exploiting temporal parallelism. However，the relationship between the quality and the number of Trotter slices is mostly unknown. In this paper, we use max-cut benchmarks to conduct a quantitative analysis to investigate the relationship between the quality and the number of Trotter slices. We found that the quality can be improved or the processing time can be reduced by temporal parallel processing of Trotter slices on FPGA accelerators.