Day 3 (Poster D)

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Title: Integer Boltzmann Machines for Future Generation Digital Annealing Units

Abstract:
Boltzmann Machines are recurrent, binary, neural networks that have been used extensively in combinatorial optimization due to their simplicity and ease of parallelization. While there exist a wide range of Boltzmann Machine based software systems, the end of Dennard Scaling has led to the increasing development of domain-specific hardware accelerators in this area, such as Fujitsu Digital Annealing Units. However, such hardware must often sacrifice the number of supported variables for connectivity and constraint support, with the latter being required to extend the hardware to support integer variables. In this presentation, we introduce a modified Boltzmann Machine algorithm for future generation Digital Annealing Units that can natively support integer variable assignment problems while reducing weight memory requirements by over 99% compared to the second generation Digital Annealing Unit. We implement a software prototype of this system in combination with a Parallel Tempering scheduling scheme using a multi-core CPU and show that it can, on average, perform over 50 times faster than the next best, published, solver system. Lastly, we give an overview of how this algorithm scales and performs when ported to custom hardware.