

Day 2

Hiroataka Tamura, DXR Laboratory Inc.

Title: Extended Ising Machine for Future DAUs

Abstract:

The core of the "Fujitsu Digital Annealer" optimization service is the DAU, a dedicated accelerator ASIC that achieves high speed through parallel processing. Common complaints about Ising machines are that the cost function is restricted to a binary quadratic form, the number of coupling topologies and variables is limited, and it is challenging to set constraints such as inequality constraints. We propose an extended Ising machine that adds an auxiliary network and control circuit to the current DAU architecture to address these complaints. With the addition of the auxiliary network, penalty terms representing inequality and equality constraints can be easily added to the ordinary quadratic form. The added networks also enable the proposed method to represent higher-order cost terms. These features can be added without changing the speed of the existing DA. We present the performance of the proposed extended Ising machine for problems involving higher-order cost functions and for applications with various constraints.

This work was done in collaboration with F. Mousavi and A. Sheikholeslami, the University of Toronto, Canada, and M. Konoshima, K. Kanda, and Aki Dote, Fujitsu Limited, Kawasaki, Japan. We are grateful to Yuuki Furue of Saitama University for developing the test codes.